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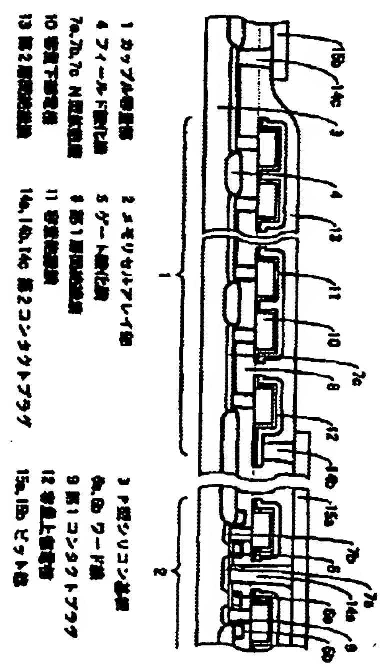
(54)【発明の名称】 半導体記憶装置

(57)【要約】

【目的】 多値メモリのセンス動作のマージンを大きく確保できるようにする。容量絶縁膜のリーク電流の抑制。最小設計寸法の維持。

【構成】 ビット線対（BL，BLB）は複数の分割ビット線対（BL1，BL1B；BL2，BL2B）に分割され、隣接する分割ビット線同士ではたすき掛けにカップル容量素子が形成される。メモリセルアレイ部2では、MOSFETと容量下部電極10、容量絶縁膜11、容量上部電極12からなるセル容量とを含むメモリセルが形成される。カップル容量部1では、分割ビット線15a（BL1）と分割ビット線15b（BL2B）との間に、セル容量と同一のプロセスで形成された単位容量素子を複数個直列に接続して構成されたカップル容量素子が接続される。分割ビット線BL1B，BL2間にも同様のカップル容量素子が形成される。



PATENT ABSTRACTS OF JAPAN

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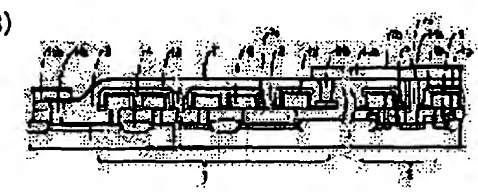
(54) SEMICONDUCTOR MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To enable a specific ratio between a coupling capacitance and a memory cell capacitance to be secured constantly by forming a coupling capacitor and a memory cell capacitor by the same process.

SOLUTION: Bit line pair (BL, BLB) are splitted into a plurality of splitted bit line pairs (BL1, BL1B; BL2, BL2B) so as to form coupling capacitor with mutually adjacent splitted bit lines tucked up. A memory cell containing a MOSFET, a capacitor lower electrode 10, a capacitor insulating film 11 and a capacitor upper electrode 12 is formed in a memory cell array part 2. A coupling capacitor composed of a plurality of unit capacitors formed in the same process as that of the cell capacitors series connected is connected between the splitted bit line 15a (BL1) and the splitted bit line (BL2B) in the coupling capacitor part 1. Likewise, the same coupling capacitor is formed between the splitted bit lines BL1B and BL2.



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[Claim(s)]

[Claim 1] It is the semiconductor memory characterized by forming two electrodes and capacity insulator layers of the aforementioned couple capacitative element in the semiconductor memory by which a bit line pair is divided into plurality and couple capacitative element is formed in tucking up its sleeves with a cord between the divided adjoining division bit lines by the conductive layer and insulator layer of the same layer as two electrodes of the capacitative element for data storages of a memory cell, and capacity insulator layers.

[Claim 2] The aforementioned couple capacitative element is a semiconductor memory according to claim 1 characterized by connecting to a serial two or more unit capacitative element which has the same layer structure as the aforementioned capacitative element for data storages.

[Claim 3] The aforementioned unit capacitative element which constitutes couple capacitative element is a semiconductor memory according to claim 2 characterized by a flat-surface configuration being equivalent to it of the aforementioned capacitative element for data storages, or forming it more widely than it.

[Claim 4] The semiconductor memory according to claim 1 characterized by forming the aforementioned couple capacitative element and the aforementioned capacitative element for data storages on bit line pair twinning.

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the multiple-value dynamic random access memory (DRAM) it was made to make one cell memorize two or more bits about a semiconductor memory.

[0002]

[Description of the Prior Art] Storage capacity (number of bits) will increase by 4 times in about three years, and dynamic random access memory is developed. Increase of such storage capacity has so far be n attained by the increase in high integration by detailed-izing of a semiconductor device, and a chip size. However, while detailed-ized

processing of a pattern becomes difficult, it is becoming still more difficult to secure the reliability of the element which turned minutely. Moreover, increase of a chip size not only causes the increase in cost, but causes the fall of the manufacture yield.

[0003] Usually, as for the memory cell, 1 bit consists of binary [of 0 level and 1 level]. Therefore, in order to increase the bit capacity of DRAM, the number of memory cells must be increased and increase of bit capacity will cause the above problems inevitably. As what solves this problem, the so-called multiple-value memory which makes the number of level of a memory cell larger than binary is proposed (JP,63-149900,A etc.).

[0004] As multiple-value memory, the sense of each bit is performed from MSB (most significant bit) one by one to LSB (least significant bit), the method which changes the sense level of a lower bit using the sense result of a high order bit is newly originated, and it is expected as what can carry out [detailed]-izing of the area per bit more as compared with the conventional multiple-value memory. The circuit diagram of the multiple-value memory is shown in drawing 4 .

[0005] a bit line pair -- BL and BLB -- the transfer gate TG -- 2 sets of division bit line pairs -- BL1 and BL1B -- And it is divided into BL2 and BL2B and each division bit line pair has sense amplifiers SA1 and SA2. an original bit line pair -- the memory cell on the intersection of BL, BLB, and a word line WLi (i= 0-255) -- a division bit line pair -- it has distributed to BL1, BL1B, and BL2 and BL2B Distribution of a memory cell is distributed so that the ratio of the stray capacity (all, such as a sense amplifier, were included) CB1 and CB2 of a division bit line may be set to 1:2.

[0006] Moreover, the couple capacitative element Cc (Cc also means the capacity value of this couple capacitative element) is respectively connected between the division bit line BL1, BL2B, and BL2 and BL1B. The memory cell is equipped with the cell capacitative element Cs (Cs also means the capacity value of this cell capacitative element), and the fixed potential VP (=1/2VCC) called plate potential is impressed to the end of Cs. Moreover, the division bit line BL1, BL2B, and BL2 and BL1B are connected to input-output-line I/O1 and I/O2 through the transistor controlled by the signal of the column selection line CSL, respectively.

[0007] Next, operation of this multiple-value memory is explained with reference to drawing 5 (a) and (b). here -- drawing 5 (a) and (b) -- respectively -- a division bit line pair -- the voltage waveform of BL2, BL2B, and division bit line pair BL1 and BL1B is shown the time of standby -- the transfer gate TG -- turning on -- **** -- a bit line pair -- BL and BLB are precharged by the precharge transistor (with no illustration), and the equalizing transistor (with no illustration) as well as the usual DRAM at 1/2VCC Then, if a word line is chosen at time T1, a cell data will be read for any of bit lines BL or BLB

being. The potential of the bit line of the side to which a selection cell is not connected stops at precharge level. Since the transfer gate is turned on at this time, even if a selection cell is in which [of a division bit line pair] side, in a biparite rate bit line, the same voltage according to "0"- "3" of a cell data appears. This voltage is lower than 1/2VCC (=VP), when cell datas are "0" and "1", as shown in drawing 5 , and when it is "2" and "3", it becomes higher than VP.

[0008] time T2 -- setting -- the transfer gate TG -- turning off -- continuing -- a sense amplifier SA 2 -- activation -- starting -- a division bit line pair -- amplification of the data on BL2 and BL2B starts time T3 -- setting -- a division bit line pair -- one side of BL2 and BL2B -- "1" -- level (VCC) and another side are set to "0" level (GND) Here, a selection cell is connected to a bit line BL side, and if it assumes that it is that by which "2" or "3" was stored in the cell, VCC level and BL2B will serve as [BL2] GND level.

[0009] At this time, the amplitude of BL2 and BL2B serves as 1/2VCC in general. Consequently, BL1B will be raised xV with the couple capacity Cc, and BL1 will be reduced xV. Here, if the couple capacity Cc is adjusted so that the potential difference of adjacent signal level may be set to 2dV(s) and it may become equal to dV about the potential difference xV to change, the level of BL1B used as reference level will serve as VP+dV from VP. On the other hand, when stored data is "2", it passes through the level of BL1 by the side of a selection cell VP from VP+dV, and when stored data is "3", it changes to VP+2dV from VP+3dV.

[0010] Therefore, if a sense amplifier SA 1 is activated at time T4, according to stored data, one side will be set to "1" level (VCC), and, as for BL1 and BL1B, another side will be set to "0" level (GND). That is, when stored data is "2", as a solid line shows, and BL1 serves as [VCC and BL1B] GND, and a dotted line shows, BL1 serves as [when stored data is "3", / GND and BL1B] VCC.

[0011] a potential change according to the couple capacity Cc when the stored data of a selection cell is "0" or "1" -- an opposite direction -- working -- the reference potential of BL1B -- VP to VP-dV -- becoming -- the level of BL1 of another side -- VP-2 -- it is set to dV (at the time of "0"), or VP (at the time of "1") Thus, it senses by SA2 and the data of LSB by SA1 by feeding back the result to the sense level of SA1 at SA2 It is amplified. [the data of MSB] These signals are read outside through I/O1 and I/O2 by making the signal of a column selection line into highness. Moreover, the re-writing to a cell can be performed by making the transfer gate TG turn on still in the state in the state where the word line WLk (k= 0, 3 [2 and 3], ...) was chosen. At this time, the potential of a bit line serves as "3" and level which sets GND to "0" in VCC decided by the potential of the bit line before ON of TG, and the capacity factor of the bit line capacity CB1 and CB2.

[0012] Since the transfer gate TG turns on the voltage difference Vr which will be read [capacity] from the cell between the highest voltage (VCC) and the minimum voltage (GND) which are stored in a cell in the capacity of BL1 of Cs and a division bit line if capacity of a memory cell is set to CB1 at the time of read-out and bit line capacity serves as 3CB(s)1 here, it is Vr=VCC/(1+3CB1/Cs).

It becomes. Since it is Vr/3, potential difference 2dV between each level is 2dV=VCC/{3 (1+3CB1/Cs)}.

It becomes.

[0013] The potential change xV given to the bit line which carried out cross intersection through the couple capacity Cc with the amplitude of VCC of a bit line on the other hand is xV=VCC/{2 (1+CB1/Cc)}.

It becomes. Therefore, the conditions for xV=dV being materialized are 1+CB1/Cc=3 (1+3CB1/Cs).

Here, since it is CB1/Cs>>1 and CB1/Cc>>1, it is set to CB1/Cc=9CB1/CsCc=Cs/9. Therefore, what is necessary will be just to set couple capacity between bit lines to one ninth of cell capacity (however, this value does not change by changing a sense method, and is not fixed).

[0014]

[Problem(s) to be Solved by the Invention] In order to mistake bits other than MSB by multiple-value memory of composition of having mentioned above and to read by it that there is nothing, it is that it is very important to fix the ratio of the couple capacity Cc and the memory cell capacity Cs. When this ratio is not regularity-ized, the tolerance to read-out voltage becomes low, and the possibility of incorrect read-out becomes high again. It will **, and cannot avoid that process change arises in a semiconductor manufacturing process, but variation will arise in the capacity value of the capacitative element formed in the process when change arose in a process. Therefore, the 1st technical problem which this invention should solve is enabling it to always secure uniformly the capacity factor of the couple capacity Cc and the memory cell capacity Cs, even if change may arise in a manufacture process. This 1st technical problem is solvable by forming couple capacitative element and memory cell capacitative element according to the same process. It is because variation can be prevented from being generated in a capacity factor if it does in this way even if variation may arise in the electrode height of the thickness of a capacity insulator layer, or capacitative element and variation may arise in capacity value by process change for the reason.

[0015] Although it is necessary to enlarge memory cell capacity Cs in order to operate DRAM stably, since the cell size became small, recently, the SUTAKKUTO type and

trench type which formed capacitor structure in three dimensions are used. Pattern formation of the electrode connected to the diffusion layer of the transistor which constitutes these capacitor structure is carried out using the lower limit called design rule. It is necessary to form the couple capacity Cc correctly so that it may always become 1/several values to the memory cell capacity Cs. by the way, for the reason Although it is desirable to form couple capacitative element and memory cell capacitative element in the same process, since memory cell capacitative element is already designed based on the minimum design rule, the material of the same layer as Cs -- using it -- in addition -- and it is very difficult to obtain several [1/] of the capacity of Cs by independent capacitative element Therefore, the 2nd technical problem which should solve this invention is enabling it to form the element of several [1/] of the capacity of cell capacity, using the material of the same layer as the cell capacity Cs maintaining the minimum design rule.

[0016] In order to enlarge memory cell capacity Cs, thickness of a capacity insulator layer is thin-film-ized by even the minimum thickness which can disregard leak in the voltage concerning a capacity film. The voltage of the potential difference between bit lines BL and BLB and a plate joins the capacity insulator layer of memory cell capacitative element. The voltage which joins a bit line changes between the supply voltage VCC inside a memory cell, and the grounding potential GND. The voltage VP which joins a plate is VCC of half of supply voltage inside memory cell/2. Therefore, the voltage impressed to the capacity insulator layer of memory cell capacitative element is VCC/2 at the maximum. On the other hand, couple capacity is connected to two bit lines which become a pair. therefore, the voltage which joins couple capacitative element -- a maximum of -- it becomes the double precision of VCC and memory cell capacitative element Therefore, the 3rd technical problem which should solve this invention is making it cause neither leak nor dielectric breakdown, even if voltage higher than memory cell capacity may be impressed to the couple capacitative element formed of the same process as memory cell capacitative element.

[0017]

[Means for Solving the Problem] The 1st technical problem mentioned above is solvable by forming couple capacitative element in the same process as memory cell capacitative element. Moreover, the above-mentioned 2nd and the 3rd technical problem can solve couple capacitative element equivalent to memory cell capacitative element, or by constituting by the series connection of two or more unit capacitative element which has the size beyond it more greatly [capacity value] on a par with memory cell capacitative element than it..

[0018]

[Embodiments of the Invention] The semiconductor memory by this invention is multiple-value memory by which a bit line pair is divided into plurality and couple capacitative element is formed in tucking up its sleeves with a cord between the divided adjoining division bit lines, and is characterized by forming two electrodes and capacity insulator layers of the aforementioned couple capacitative element by the conductive layer and insulator layer of the same layer as two electrodes of the capacitative element for data storages (memory cell capacitative element), and capacity insulator layers.

[0019] And preferably, the aforementioned couple capacitative element has the same layer structure as the aforementioned memory cell capacitative element, to this, or two or more large unit capacitative element is connected to a serial, and a flat-surface configuration consists of this.

[0020] According to the above-mentioned composition, even if variation may arise in the capacity value of the formed capacitative element by metaphor process change, since the variation appears with the same inclination by couple capacity and memory cell capacity, it does not affect a capacity factor. Moreover, since it is not necessary to establish the special process for forming couple capacity according to this invention, the secondary effect that multiple-value memory can be formed according to the same simple process as the case where the conventional DRAM of 1 bit of one cell is manufactured is also enjoyable.

[0021] Moreover, it is the same as the size of memory cell capacitative element in couple capacitative element, or it becomes possible to form the capacitative element of the capacity value below memory cell capacity, without reducing the minimum design size used when forming a memory cell, since two or more unit capacitative element of the size beyond it is connected to a serial and it constitutes. Furthermore, even if the voltage impressed to each unit capacitative element by having constituted couple capacitative element with the series-connection object of two or more unit capacitative element is divided, the voltage which joins the capacity insulator layer is set to 1 for the series-connection number of voltage which joins a bit line and the voltage more than a memory cell may be impressed to couple capacity, it is lost that big leak flows to the capacity insulator layer, or dielectric breakdown arises.

[0022]

[Example] Next, the example of this invention is explained with reference to a drawing.

[1st example] drawing 1 is the circuit diagram showing the 1st example of this invention. A different point from the circuit shown in drawing 4 is a point which connects to a serial two or m re unit capacitative element which is connected between

the division bit line BL1, BL2B, and BL2 and BL1B, and in which the couple capacitative element Cc has the same layer structure as the memory cell capacitative element Cs, and is constituted respectively. Since the other point and circuit operation are the same as that of the case of the circuit shown in drawing 4 , the detailed explanation is omitted. Specifically in the circuit shown by drawing 1 , the series connection of the nine unit capacitative element is carried out. This number changes according to the capacity value of unit capacitative element, and the kind of sense circuit.

[0023] Drawing 2 is the cross section having shown typically the structure of the couple part by volume 1 in the semiconductor device of the 1st example of this invention, and the memory cell array section 2. As shown in drawing 2 , the gate oxide film 5 is formed in the front face of the P type silicon substrate 3 separated by the isolation field which consists of a field oxide film 4. On the field oxide film 4 and the gate oxide film 5, word lines 6a and 6b are formed. The portion on the gate oxide film 5 of a word line constitutes the gate electrode.

[0024] In the surface field of the P type silicon substrate 3 of the memory cell array sections 2 other than the field in which the field oxide film 4 and the gate electrode (6a) are formed, the N type diffusion layers 7a and 7b used as the source drain field of a transistor are formed, and N type diffusion layer 7c for connecting unit capacitative element is formed in the front face of the P type silicon substrate 3 of the couple part by volume 1. On these front faces, while [the 1st layer] consisting of a silicon oxide, the insulator layer 8 has accumulated. Into the insulator layer 8, the 1st contact plug 9 which connects with N type diffusion layer 7b the capacity lower electrode 10 formed on the insulator layer 8 between the 1st layer is formed between the 1st layer.

[0025] The capacity up electrode 12 is formed through the capacity insulator layer 11 deposited on the front face on the capacity lower electrode 10. The insulator layer 13 has accumulated between the 2nd layer on the insulator layer 8 and the capacity up electrode 12 between the 1st layer. Into the insulator layer 13, 2nd contact plug 14b which connects the capacity up electrode 12 and bit line 15a formed on the insulator layer 13 between the 2nd layer is formed between the 2nd layer. Into the insulator layer 8 and the insulator layer 13 between the 2nd layer, the 2nd contact plugs 14a and 14c which connect the N type diffusion layers 7a and 7c and the bit lines 15a and 15b formed on the insulator layer 13 between the 2nd layer are formed between the 1st layer. Consequently, the memory cell of the SUTAKKUTO capacitor structure where the capacitative element of the memory cell which consisted of a capacity lower electrode 10, a capacity insulator layer 11, and a capacity up electrode 12 is formed in the lower part

of bit line 15a in the upper part of word line 6a is formed in the memory cell array section 2.

[0026] Moreover, the unit capacitative element [two or more (here nine pieces)] which consisted of a capacity lower electrode 10, a capacity insulator layer 11, and a capacity up electrode 12 is formed in the couple part by volume 1. Each unit capacitative element reaches capacity up electrode 12, and is connected in series with the 1st contact plug 9 by N type diffusion layer 7c. The end connected in series is connected to bit line 15b through [becoming a pair] 2nd contact plug 14b, and the other end is connected to bit line 15b of another side which becomes a pair through 2nd contact plug 14c. Therefore, the couple capacitative element which consists of a series-connection object of unit capacitative element between bit line 15a and 15b is connected. In the couple part by volume 1, all unit capacitative element is designed so that it may have a capacity equivalent to the cell capacity Cs of a memory cell.

[0027] [2nd example] drawing 3 is the cross section having shown typically the structure of the couple part by volume 21 in the semiconductor device of the 2nd example of this invention, and the memory cell array section 22. In addition, the circuit diagram of this example memory is the same as that of the thing of the 1st example shown in drawing 1 . As shown in drawing 3 , the gate oxide film 25 is formed in the front face of the P type silicon substrate 23 separated by the isolation field which consists of a field oxide film 24. Word line 26a formed in the field of the request on the gate oxide film 25 constitutes the gate electrode of a transistor, and word line 26b formed on the field oxide film 24 has become the wiring which connects a gate electrode. In the surface field of the P type silicon substrate 23 of the memory cell array sections 22 other than the field in which the field oxide film 24 and the gate electrode (26a) are formed, the N type diffusion layers 27a and 27b used as the source drain of a transistor are formed, and N type diffusion layer 27c for connecting a capacitor is formed in the front face of the P type silicon substrate 23 of the couple part by volume 21. On these front faces, while [the 1st layer] consisting of a silicon oxide, the insulator layer 28 has accumulated.

[0028] Into the insulator layer 28, the 1st contact plug 29 which connects N type diffusion layer 27b and bit line 30a formed on the insulator layer 28 between the 1st layer is formed between the 1st layer. On the front face of bit lines 30a and 30b, and the insulator layer 28 between the 1st layer, the insulator layer 31 has accumulated between the 2nd layer. Into the insulator layer 31, 2nd contact plug 32c which connects bit lines 30a and 30b and the capacity lower electrode 33 formed on th insulator layer 31 between the 2nd layer is formed between the 2nd layer. Into the insulator layer 28

and the insulator layer 31 between the 2nd layer, the 2nd contact plugs 32a and 32b which connect the N type diffusion layers 27b and 27c and the capacity lower electrode 33 formed on the insulator layer 31 between the 2nd layer are formed between the 1st layer.

[0029] On the capacity lower electrode 33, the capacity up electrode 35 is formed through the capacity insulator layer 34 deposited on the front face. Consequently, the memory cell of the SUTAKKUTO capacitor structure where the capacitative element of the memory cell which consisted of a capacity lower electrode 33, a capacity insulator layer 34, and a capacity up electrode 35 is formed in word line 26a and the bit line 30a upper part is formed in the memory cell array section 22. Moreover, the capacitor [two or more (this example 12 pieces)] which consisted of a capacity lower electrode 33, a capacity insulator layer 34, and a capacity up electrode 35 is formed in the couple part by volume 21. Each capacitor reaches capacity up electrode 35, and is connected in series by 2nd contact plug 32b and N type diffusion layer 27c. The end connected in series is connected to bit line 30a through [becoming a pair] 2nd contact plug 32c, and the other end is connected to bit line 30b of another side which becomes a pair through 2nd contact plug 32c. Therefore, between bit line 30a and 30b, it means that the couple capacitative element constituted with the series-connection object of unit capacitative element was connected. In this example, the couple capacitative element of the capacity value of Cs/9 has been obtained by carrying out the 12-piece series connection of the unit capacitative element which has 4/3 of the capacity of the memory cell capacity Cs.

[0030]

[Effect of the Invention] Since the semiconductor memory by this invention forms the couple capacitative element between bit lines in the same process as memory cell capacitative element as it connected above, even if variation arises in for example, capacity insulation thickness, electrode height, etc., since the ratio of the capacity of a memory cell and couple capacity is kept constant by change of the process at the time of forming capacity even if, it can secure the margin of multiple-value sense operation greatly by it. Moreover, since the same layer as the layer which constitutes memory cell capacitative element is used for the electrode layer and capacity insulator layer which constitute couple capacitative element, it is not necessary to increase a manufacturing process and they can manufacture multiple-value memory with a manufacturing cost equivalent to the conventional DRAM.

[0031] Moreover, it becomes possible about couple capacitative element equivalent to memory cell capacitative lem nt, or to form the couple capacitative element of the capacity value below memory cell capacity, maintaining the minimum design size used

とが可能になる。そして、最小設計寸法に変更がないため、新たな製造装置を投入する必要はなく設備コストの負担を増加させることなく、多値メモリの製造が可能になる。

【0032】さらに、カップル容量素子が複数個の単位容量素子の直列接続体により構成されていることにより、全体にかかる電圧は分割され、個々の単位容量素子の容量絶縁膜にかかる電圧がビット線にかかる電圧の直列接続個数分の１になり、メモリセル容量素子に用いる容量絶縁膜と同じ絶縁膜を用いても、リーク電流が増加したり絶縁破壊が生じたりすることはなく、高い信頼性を維持することができる。

【図面の簡単な説明】

【図１】本発明の第１の実施例の回路図。

【図２】本発明の第１の実施例の断面図。

【図３】本発明の第２の実施例の断面図。

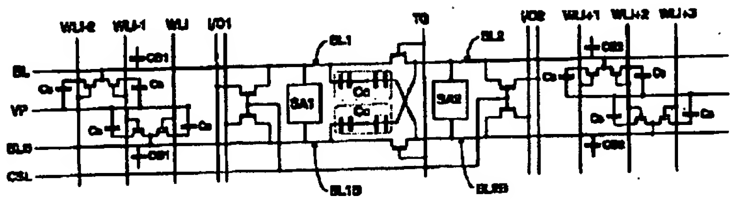
【図４】本発明に先行して創案された多値メモリの回路図。

【図５】図４に示した多値メモリの動作説明図。

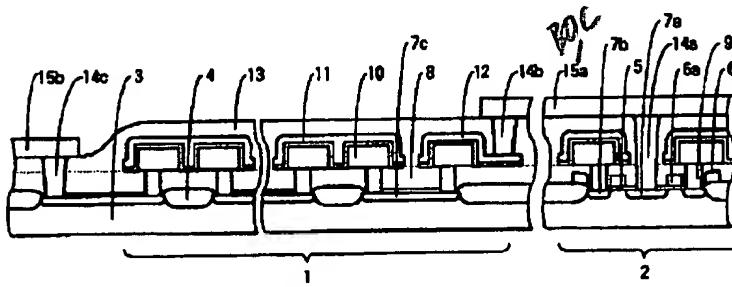
【符号の説明】

１、２１　カップル容量部
２、２２　メモリセルアレイ部
３、２３　Ｐ型シリコン基板
４、２４　フィールド酸化膜
５、２５　ゲート酸化膜
６ａ、６ｂ、２６ａ、２６ｂ　ワード線
７ａ、７ｂ、７ｃ、２７ａ、２７ｂ、２７ｃ　Ｎ型拡散層
８、２８　第１層間絶縁膜
９、２９　第１コンタクトプラグ
１０、３３　容量下部電極
１１、３４　容量絶縁膜
１２、３５　容量上部電極
１３、３１　第２層間絶縁膜
１４ａ、１４ｂ、１４ｃ、３２ａ、３２ｂ、３２ｃ　第２コンタクトプラグ
１５ａ、１５ｂ、３０ａ、３０ｂ　ビット線

【図１】

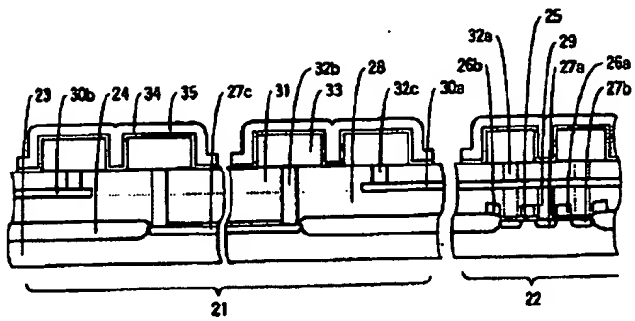


【図２】



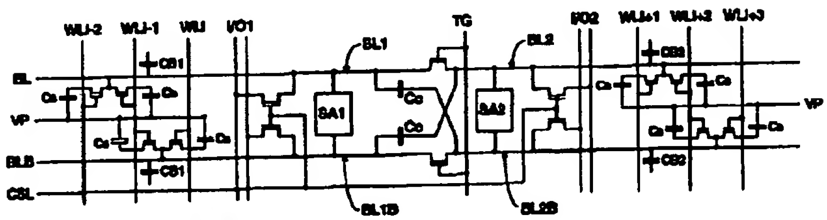
1 カップル容量部　2 メモリセルアレイ部　3 P型シリコン基板
4 フィールド酸化膜　5 ゲート酸化膜　6a,6b ワード線
7a,7b,7c N型拡散層　8 第1層間絶縁膜　9 第1コンタクトプラグ
10 容量下部電極　11 容量絶縁膜　12 容量上部電極
13 第2層間絶縁膜　14a,14b,14c 第2コンタクトプラグ　15a,15b ビット線

【図3】



21 カップル容量部
22 メモリセルアレイ部
23 P型シリコン基板
24 フィールド酸化膜
25 ゲート酸化膜
26a, 26b ワード線
27a, 27b, 27c N型拡散層
28 第1層間絶縁膜
29 第1コンタクトプラグ
30a, 30b ビット線
31 第2層間絶縁膜
32a, 32b, 32c 第2コンタクトプラグ
33 容量下部電極
34 容量絶縁膜
35 容量上部電極

【図4】



【図5】